IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

ERNST BRETSCHNEIDER ET AL DE 010005

Serial No.

Filed: CONCURRENTLY

CIRCUIT ARRANGEMENT AND METHOD OF PROTECTING AT LEAST A CHIP ARRANGEMENT FROM MANIPULATION AND/OR ABUSE

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. A circuit arrangement (100) as claimed in claim 1, characterized in that the detector unit (10) comprises at least one bipolar transistor (12), particularly at least one pnp transistor.

5. A circuit arrangement (100) as claimed in claim 3, characterized in that the emitter (124) of the bipolar transistor (12) is connected to the input (22), provided for the output voltage (V_{out}), of the comparator unit (20).

6. A circuit arrangement (100) as claimed in claim 3, characterized in that the emitter (124) of the bipolar

transistor (12) is connected to at least a power supply voltage (V_{dd}) via at least a power supply resistor (14).

7. A circuit arrangement (100) as claimed in claim 3, characterized in that the collector (126) of the bipolar transistor (12) is connected to ground potential via at least a reference resistor (16).

8. A circuit arrangement (100) as claimed in claim 3, characterized in that the junction between the base (122) of the bipolar transistor (12) and the collector (126) of the bipolar transistor (12) is provided for absorbing the light incident on the detector unit (10).

9. A circuit arrangement (100) as claimed in claim 1, characterized in that the output voltage (V_{out}) of the detector unit (10) depends on the wavelength and/or the intensity of the incident light (Li).

10. A circuit arrangement (100) as claimed in claim 1, characterized in that

at least an evaluation unit (30) is implemented and/or integrated in the comparator unit (20), or

the comparator unit (20) precedes at least an evaluation unit (30).

12. A circuit arrangement (100) as claimed in claim 1, characterized in that

the working point of the detector unit (10) and/or

the threshold value of the reference voltage (V_{ref}) is adjustable.

13. A circuit arrangement (100) as claimed in claim 1, characterized in that at least a dielectric coating, particularly an insulation layer and/or passivation layer

and/or a further protective coating which is provided for protecting the chip arrangement (200) from external influences and preferably cannot be easily removed is arranged within the chip arrangement (200) and/or laterally to the chip arrangement (200) and/or on the chip arrangement (200).

15. A circuit arrangement (100) as claimed in claim 13, characterized in that the material of the dielectric coating is substantially opaque.

16. A circuit arrangement (100) as claimed in claim 1, characterized in that the chip arrangement (200) is arranged on at least a particularly layered carrier substrate of a semiconducting or insulating material.

17. A circuit arrangement (100) as claimed in claim 1, characterized in that the circuit arrangement (100) is implemented and/or integrated in at least a card, particularly in at least a chip card or in at least a smart card.

18. A card, particularly a chip card or smart card, comprising at least an electric or electronic circuit arrangement (100) as claimed in claim 1.

19. A chip arrangement (200), for example a (semiconductor) chip arrangement, particularly a controller chip arrangement for a chip card or smart card, the chip arrangement comprising

at least one, preferably a plurality or a large number of particularly optosensitive detector units (10) as claimed in claim 1, and

at least a combination logic unit (40) for combining the detector units (10).

21. A chip arrangement (200) as claimed in claim 19, characterized in that the combination logic unit (40) is connected to at least a particularly electrically erasable storage unit (60).

23. A chip arrangement (200) as claimed in claim 20, characterized in that

the storage unit (60) is arranged between the combination logic unit (40) and the control logic unit (50), and

the access to the data and/or functions of the chip arrangement (200) to be protected can be blocked by blocking (S) the storage unit (60) when a failure message occurs particularly during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

24. A chip arrangement (200) as claimed in claim 19, characterized in that the chip arrangement (200) can be permanently short-circuited via the power supply voltage (V_{dd}), particularly via the power supply terminals of the chip arrangement (200).

27. A method as claimed in claim 25, characterized in that the failure message is triggered in the comparator unit (20) when the output voltage (V_{out}) of the detector unit (10) deviates from the nominal range.

28. A method as claimed in claim 25, characterized in that the triggering of the failure message is adjusted by means of

the working point of the detector unit (10) and/or

the threshold value of the reference voltage (V_{ref}).

29. A method as claimed in claim 25, characterized in that the failure message is generated in at least

an evaluation unit (30) implemented and/or integrated in the comparator unit (20), or

an evaluation unit (30) preceded by the comparator unit (20).

30. A method as claimed in claim 25, characterized in that at least a control logic unit (50) connected to at least a combination logic unit (40) provided for combining the detector units (10) is temporarily blocked (S) when the failure message is triggered.

31. A method as claimed in claim 25, characterized in that at least an electrically erasable storage unit (60) arranged between at least a combination logic unit (40) provided for combining the detector units (10) and at least a control logic unit (50) is permanently blocked (S) when the failure message is triggered.

33. A method as claimed in claim 25, characterized in that a particularly once-electrically programmable storage unit (60) connected to at least a combination logic unit (40) provided for combining the detector units (10) is permanently blocked (S) when the failure message is triggered.

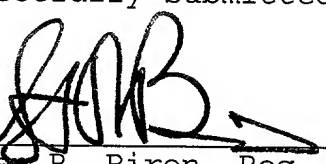
35. A method as claimed in claim 25, characterized in that the data and/or functions to be protected are erased (L) in an EEPROM storage unit (60') (EEPROM = Electrically Erasable Programmable Read-Only Memory) connected to at least a combination logic unit (40) provided for combining the detector units (10) when the failure message is triggered.

REMARKS

The foregoing amendments to claims 3, 5-10, 12-13, 15-19, 21, 23-24, 27-31, 33 and 35, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By 
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APPENDIX

3. A circuit arrangement (100) as claimed in claim 1 ~~or 2~~, characterized in that the detector unit (10) comprises at least one bipolar transistor (12), particularly at least one pnp transistor.

5. A circuit arrangement (100) as claimed in claim 3 ~~any one of claims 3 to 4~~, characterized in that the emitter (124) of the bipolar transistor (12) is connected to the input (22), provided for the output voltage (V_{out}), of the comparator unit (20).

6. A circuit arrangement (100) as claimed in claim 3 ~~any one of claims 3 to 5~~, characterized in that the emitter (124) of the bipolar transistor (12) is connected to at least a power supply voltage (V_{dd}) via at least a power supply resistor (14).

7. A circuit arrangement (100) as claimed in claim 3 ~~any one of claims 3 to 6~~, characterized in that the collector (126) of the bipolar transistor (12) is connected to ground potential via at least a reference resistor (16).

8. A circuit arrangement (100) as claimed in claim 3 ~~any one of claims 3 to 7~~, characterized in that the junction between the base (122) of the bipolar transistor (12) and the collector (126) of the bipolar transistor (12) is provided for absorbing the light incident on the detector unit (10).

9. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 8~~, characterized in that the output voltage (V_{out}) of the detector unit (10) depends on the wavelength and/or the intensity of the incident light (Li).

10. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 9~~, characterized in that

at least an evaluation unit (30) is implemented and/or integrated in the comparator unit (20), or

the comparator unit (20) precedes at least an evaluation unit (30).

12. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 11~~, characterized in that

the working point of the detector unit (10) and/or

the threshold value of the reference voltage (V_{ref}) is adjustable.

13. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 12~~, characterized in that at least a dielectric coating, particularly an insulation layer and/or passivation layer and/or a further protective coating which is provided for protecting the chip arrangement (200) from external influences and preferably cannot be easily removed is arranged within the chip arrangement (200) and/or laterally to the chip arrangement (200) and/or on the chip arrangement (200).

15. A circuit arrangement (100) as claimed in claim 13 ~~or 14~~, characterized in that the material of the dielectric coating is substantially opaque.

16. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 15~~, characterized in that the chip arrangement (200) is arranged on at least a particularly layered carrier substrate of a semiconducting or insulating material.

17. A circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 16~~, characterized in that the circuit

arrangement (100) is implemented and/or integrated in at least a card, particularly in at least a chip card or in at least a smart card.

18. A card, particularly a chip card or smart card, comprising at least an electric or electronic circuit arrangement (100) as claimed in claim 1 ~~any one of claims 1 to 17~~.

19. A chip arrangement (200), for example a (semiconductor) chip arrangement, particularly a controller chip arrangement for a chip card or smart card, the chip arrangement comprising

at least one, preferably a plurality or a large number of particularly optosensitive detector units (10) as claimed in claim 1 ~~any one of claims 1 to 20~~, and

at least a combination logic unit (40) for combining the detector units (10).

21. A chip arrangement (200) as claimed in claim 19 ~~or 20~~, characterized in that the combination logic unit (40) is connected to at least a particularly electrically erasable storage unit (60).

23. A chip arrangement (200) as claimed in claim 20, ~~21 or 22,~~ characterized in that

the storage unit (60) is arranged between the combination logic unit (40) and the control logic unit (50), and

the access to the data and/or functions of the chip arrangement (200) to be protected can be blocked by blocking (S) the storage unit (60) when a failure message occurs particularly during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).

24. A chip arrangement (200) as claimed in claim 19 ~~any one of claims 19 to 23~~, characterized in that the chip arrangement (200) can be permanently short-circuited via the power supply voltage (V_{dd}), particularly via the power supply terminals of the chip arrangement (200).

27. A method as claimed in claim 25 ~~or 26~~, characterized in that the failure message is triggered in the comparator unit (20) when the output voltage (V_{out}) of the detector unit (10) deviates from the nominal range.

28. A method as claimed in claim 25 ~~any one of claims 25 to 27~~, characterized in that the triggering of the failure message is adjusted by means of

the working point of the detector unit (10) and/or

the threshold value of the reference voltage (V_{ref}).

29. A method as claimed in claim 25 ~~any one of claims 25 to 28~~, characterized in that the failure message is generated in at least

an evaluation unit (30) implemented and/or integrated in the comparator unit (20), or

an evaluation unit (30) preceded by the comparator unit (20).

30. A method as claimed in claim 25 ~~any one of claims 25 to 29~~, characterized in that at least a control logic unit (50) connected to at least a combination logic unit (40) provided for combining the detector units (10) is temporarily blocked (S) when the failure message is triggered.

31. A method as claimed in claim 25 ~~any one of claims 25 to 29~~, characterized in that at least an electrically erasable storage unit (60) arranged between at least a combination logic unit (40) provided for combining the

detector units (10) and at least a control logic unit (50) is permanently blocked (S) when the failure message is triggered.

33. A method as claimed in claim 25 ~~any one of claims 25 to 29~~, characterized in that a particularly once-electrically programmable storage unit (60) connected to at least a combination logic unit (40) provided for combining the detector units (10) is permanently blocked (S) when the failure message is triggered.

35. A method as claimed in claim 25 ~~any one of claims 25 to 29~~, characterized in that the data and/or functions to be protected are erased (L) in an EEPROM storage unit (60') (EEPROM = Electrically Erasable Programmable Read-Only Memory) connected to at least a combination logic unit (40) provided for combining the detector units (10) when the failure message is triggered.